TITLE OF THE INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING LATCHING MEANS
CAPABLE OF SCANNING

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the
benefit of priority from the prior Japanese Patent
Application No. 2001-304750, filed September 28, 2001,
the entire contents of which are incorporated herein by
reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor
integrated circuit having a latching means capable of
scanning.

2. Description of the Related Art

In synchronous semiconductor integrated circuits
which have been more and more complicated, the recent
most popular technique is to use a latching circuit
(scan chain) capable of scanning to test this latching
circuit by separating only a certain function, thereby
greatly reducing the test time. The latching means
(scan chain) capable of scanning is a means in which a
plurality of registers and the like are connected into
one or a plurality of chains so that data stored in a
preceding register can be shifted (scanned) to a
succeeding register.

In particular, a macro cell for forming an

embedded memory containing both a memory circuit and logic circuit has a large number of input/output terminals. Hence, it is essential to include the scanning function as described above to improve the fault detection ratio of the whole semiconductor integrated circuit (semiconductor chip).

FIG. 1 is a schematic view showing a method of realizing scan in a conventional macro cell. This macro cell 101 is for forming an embedded memory or the like. As shown in FIG. 1, the macro cell 101 has a large number of input/output terminals (to be referred to as IO terminals hereinafter) 102, so these IO terminals 102 are arranged with a spatial extension. Each IO terminal 102 has an input/output register (to be referred to as an IO register hereinafter) 103. These IO registers 103 have a scanning function to test data (an external path) input from the outside of this macro cell, and are connected in series.

A scan input terminal 104 is connected to one end of these IO registers 103. A scan output terminal 105 is connected to the other end of the IO registers 103. Data SI to be scanned is input to the input terminal 104, and scanned data SO is output from the scan output terminal 105. Although not shown, scan is executed by using a control input signal and a clock signal in addition to these data.

FIG. 2 is a view showing the arrangement of a

conventional embedded memory macro. An example of the realization of scan in this embedded memory macro will be described below.

As shown in FIG. 2, this embedded memory macro 111 has the macro cell 101 shown in FIG. 1, an operation control circuit 112, and a macro cell 101B. This macro cell 101B is the mirror inversion of the macro cell 101 with respect to the operation control circuit 112. In an embedded memory macro, to increase the memory capacity and share the operation control circuit 112, the macro cells 101 and 101B are usually so arranged as to have a mirror inversion relationship on the two sides of the operation control circuit 112.

In each of the macro cells 101 and 101B, 128 IO registers and 128 IO terminals are arranged. At the right end of the macro cell 101, a scan input terminal 104 connected to the right end of the IO registers is formed. At the left end of the macro cell 101, a scan output terminal 105 connected to the left end of the IO registers is formed.

The operation control circuit 112 has an input/output line for inputting and outputting a control signal CNT and has a register for storing this control signal CNT. At the right end of the operation control circuit 112, a scan input terminal 113 connected to the register is formed. At the lower end of the operation control circuit 112, a scan output

terminal 114 connected to the register is formed.

At the left end of the macro cell 101B, a scan
input terminal 104B connected to the left end of the IO
registers is formed. At the right end of the macro
5   cell 101B, a scan output terminal 105B connected to the
right end of the IO registers is formed. In addition,
the scan output terminal 114 and the scan input
terminal 104B are connected by a line 115.

The memory macro 111 configured as shown in FIG. 2
10   can achieve a memory macro scanning function by
inputting data SI to be scanned to the scan input
terminal 104 at the right end, and outputting scanned
data SO from the scan output terminal 105B.

Unfortunately, the line 115 between the scan
15   output terminal 114 and the scan input terminal 104B is
a long line extending over the 128 IO terminals, and
therefore deteriorates the performance of the scan
operation. Also, this line 115 must be formed outside
the memory macro. This interferes with automatization
20   of the scan operation.

BRIEF SUMMARY OF THE INVENTION

A semiconductor device according to an aspect of
the present invention comprises: circuits having a
certain function; a plurality of input terminals which
25   receive input data to the circuits from the outside; a
plurality of output terminals which output data output
from the circuits to the outside; a plurality of first

registers connected in series, the plurality of first registers shifting stored data to respective adjacent registers in sequence, and the plurality of first registers being connected in one-to-one correspondence to the plurality of input terminals or to the plurality of output terminals; a plurality of second registers connected in series, the plurality of second registers shifting stored data to respective adjacent registers in sequence, and the plurality of second registers being connected in one-to-one correspondence to the plurality of input terminals or to the plurality of output terminals; a first scan input terminal formed at one end of the plurality of first series-connected registers; a first scan output terminal formed at the other end of the plurality of first series-connected registers; a second scan input terminal formed at one end of the plurality of second series-connected registers; a second scan output terminal formed at the other end of the plurality of second series-connected registers; and an operation control circuit which controls operations of the circuits and the plurality of first and second registers.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a diagram showing a method of realizing scan in a conventional array block;

FIG. 2 is a diagram showing the arrangement of a conventional memory macro;

FIG. 3 is a diagram showing an array block which configures a semiconductor integrated circuit of the first embodiment of the present invention;

FIG. 4 is a diagram showing a memory macro which configures a semiconductor integrated circuit of the first modification of the first embodiment;

FIG. 5 is a diagram showing a memory macro which configures a semiconductor integrated circuit of the second modification of the first embodiment;

FIG. 6 is a diagram showing a memory macro which configures a semiconductor integrated circuit of the third modification of the first embodiment;

FIG. 7 is a diagram showing an array block which configures a semiconductor integrated circuit of the second embodiment of the present invention;

FIG. 8 is a diagram showing an array block which configures a semiconductor integrated circuit of the third embodiment of the present invention;

FIG. 9 is a diagram showing a memory macro which configures a semiconductor integrated circuit of the first modification of the third embodiment;

FIG. 10 is a diagram showing a memory macro which configures a semiconductor integrated circuit of the second modification of the third embodiment;

FIG. 11 is a diagram showing an array block which configures a semiconductor integrated circuit of the fourth embodiment of the present invention; and

FIG. 12 is a diagram showing the installation locations of scan IO terminals applicable to each embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

5   Embodiments of the present invention will be described below with reference to the accompanying drawing.   In the following explanation, the same reference numerals denote the same parts throughout the drawing.

10   First Embodiment

First, an array block constructing a semiconductor integrated circuit of the first embodiment of the present invention will be described below.

FIG. 3 is a diagram showing the arrangement of the

15   array block of the first embodiment.

As shown in FIG. 3, in this array block 11, a memory cell array 12, a row decoder 13, a column decoder 14, a sense amplifier 15, and an input/output control circuit 16 are formed.

20   In the memory cell array 12, memory cells for storing data are arrayed in a matrix manner in the row and column directions.   To select a memory cell in the row direction on the basis of an externally input row address, the row decoder 13 selects a word line WL

25   connected to the memory cell.   The sense amplifier 15 amplifies a voltage read out from the memory cell selected on the basis of the row decoder 13.   To select

a memory cell in the column direction on the basis of
an externally input column address, the column decoder
14 selects a bit line connected to the memory cell, and
connects this bit line to a DQ line. In data read, the
input/output control circuit 16 transfers data stored
in a memory cell to an output terminal. In data write,
the input/output control circuit 16 transfers data
input to an input terminal to a memory cell.

In this input/output control circuit 16,
input/output registers and scan registers (to be
referred to as IO registers hereinafter) 16A,
input/output terminals (to be referred to as IO
terminals hereinafter) 16B, a first scan input terminal
SIR1, a second scan input terminal SIL1, a first scan
output terminal SOL1, and a second scan output terminal
SOR1 are arranged.

The first scan input terminal SIR1 is placed at
the right end of the input/output control circuit 16.
The first scan output terminal SOL1 is placed at the
left end of the input/output circuit 16. The
series-connected IO registers 16A are arranged between
the first scan input terminal SIR1 and the first scan
output terminal SOL1. These IO registers 16A have
latching means capable of scanning, respectively, and
are connected in series to form a scan chain. The
IO terminal 16B is connected to each of these IO
registers 16A.

The second scan input terminal SIL1 is placed at the left end of the input/output control circuit 16. The second scan output terminal SOR1 is placed at the right end of the input/output control circuit 16. The series-connected IO registers 16A are arranged between the second scan input terminal SIL1 and the second scan output terminal SOR1. These IO registers 16A have latching means capable of scanning, respectively, and are connected in series to form a scan chain. The IO terminal 16B is connected to each of these IO registers 16A. Note that the second scan input terminal SIL1 is placed near the first scan output terminal SOL1, and the second scan output terminal SOR1 is placed near the first scan input terminal SIR1.

In addition, a line 17 is connected between the first scan output terminal SOL1 and the second scan input terminal SIL1.

In the array block 11 having this configuration, input data to the scan input terminal SIR1 is scanned in the series-connected IO registers 16A in sequence, and transferred to the scan output terminal SOL1. The data transferred to the scan output terminal SOL1 is input to the scan input terminal SIL1 through the line 17. This data input to the scan input terminal SIL1 is scanned in the IO registers 16A in sequence and transferred to the scan output terminal SOR1.

As described above, the scan input terminal SIR1

is placed at the right end of the array block 11, and
the scan output terminal SOL1 as an output of this scan
input terminal SIR1 is placed at the left end of the
array block 11. Also, the scan input terminal SIL1 is
placed at the left end of the array block 11, and the
scan output terminal SOR1 as an output of this scan
input terminal SIL1 is placed at the right end of the
array block 11. The scan output terminal SOL1 and the
scan input terminal SIL1 arranged at the left end of
the array block 11 are connected by the line 17.
Accordingly, a scan chain can be formed between the
scan input terminal SIR1 and the scan output terminal
SOR1, so data input to the scan input terminal SIR1 can
be scanned to the scan output terminal SOR1.

The line 17 cannot be a long line because it
connects the scan output terminal SOL1 and the scan
input terminal SIL1 arranged close to each other.
Therefore, even when data input to the scan input
terminal SIR1 is scanned to the scan output terminal
SOR1, deterioration of the performance of the scan
operation can be reduced.

In data read, an output from the sense amplifier
15 is stored in the IO register 16A through the DQ
line, and output to the outside from the IO terminal
16B. In data write, data externally input to the IO
terminal 16B is stored in the IO register 16A, and
written in a selected memory cell through the DQ line.

The arrangement of a memory macro in which an operation control circuit is formed in the array block 11 will be described below.

FIG. 4 is a diagram showing the arrangement of a memory macro of the first modification of the first embodiment described above.

As shown in FIG. 4, this memory macro has the array block 11 shown in FIG. 3 and an operation control circuit 21. The internal configuration of the array block 11 is the same as shown in FIG. 3. FIG. 4 shows only the scan input terminals SIR1 and SIL1 and the scan output terminals SOL1 and SOR1 in the input/output control circuit 16. In this input/output control circuit of the array block 11, 128 IO registers and 128 IO terminals are arranged.

That is, the scan input terminal SIR1 is placed at the right end of the input/output control circuit of the array block 11. The scan output terminal SOL1 is placed at the left end of this input/output control circuit. 64 series-connected IO registers are arranged between the scan input terminal SIR1 and the scan output terminal SOL1. These 64 IO registers have latching means capable of scanning, respectively, and thereby form a scan chain. An IO terminal is connected to each of these 64 IO registers.

The scan input terminal SIL1 is placed at the left end of the input/output control circuit. The scan

output terminal SOR1 is placed at the right end of the input/output control circuit. 64 series-connected IO registers are arranged between the scan input terminal SIL1 and the scan output terminal SOR1. These 64 IO registers have latching means capable of scanning, respectively, and thereby form a scan chain. An IO terminal is connected to each of these 64 IO registers.

In addition, a scan input terminal SIR2 connected to the scan output terminal SOL1 is placed at the right end of the operation control circuit 21. A scan output terminal SOL2 is placed at the left end of the operation control circuit 21. A plurality of IO registers are arranged between the scan input terminal SIR2 and the scan output terminal SOL2. These IO registers have latching means capable of scanning, respectively, and thereby form a scan chain. An IO terminal is connected to each of these IO registers.

A scan input terminal SIL2 is placed at the left end of the operation control circuit 21. A scan output terminal SOR2 connected to the scan input terminal SIL1 is placed at the right end of the operation control circuit 21. A plurality of IO registers are arranged between the scan input terminal SIL2 and the scan output terminal SOR2. These IO registers have latching means capable of scanning, respectively, and thereby form a scan chain. An IO terminal is connected to each of these IO registers. A control signal CNT is input

to and output from this IO terminal. Externally input control signals CNT include a clock signal and command signal. On the basis of an externally input clock signal, the operation control circuit 21 generates a clock signal to be used internally. Also, the operation control circuit 21 generates various operation signals on the basis of a command signal, and outputs these operation signals to the row decoder 13, the column decoder 14, and the input/output control circuit 16. That is, this operation control circuit 21 controls the operations of the row decoder 13, the column decoder 14, and the input/output control circuit 16 in accordance with an externally input clock signal and command signal.

Furthermore, a line 22 is connected between the scan output terminal SOL2 and the scan input terminal SIL2.

In the memory macro having this configuration, input data to the scan input terminal SIR1 is scanned in a plurality of series-connected IO registers in sequence, transferred to the scan output terminal SOL1, and then to the scan input terminal SIR2. The data transferred to the scan input terminal SIR2 is scanned in a plurality of IO registers and transferred to the scan output terminal SOL2.

The data transferred to the scan output terminal SOL2 is input to the scan input terminal SIL2 through

the line 22. This data input to the scan input
terminal SIL2 is scanned in a plurality of IO
registers, transferred to the scan output terminal
SOR2, and then to the scan input terminal SIL1. The
5   data input to the scan input terminal SIL1 is scanned
in a plurality of series-connected IO registers in
sequence, and transferred to the scan output terminal
SOR1.

As described above, one scan input terminal and
10   one scan output terminal are arranged at the left end
of each of the array block 11 and the operation control
circuit 21. One scan input terminal and one scan input
terminal are also arranged at the right end of each of
the array block 11 and the operation control circuit
15   21. When the array block 11 and the operation control
circuit 21 are juxtaposed, the scan output terminal
SOL1 and the scan input terminal SIR2 are connected,
and the scan output terminal SOR2 and the scan input
terminal SIL1 are connected. Accordingly, even when a
20   memory macro is constructed by the array block 11 and
the operation control circuit 21, one scan input
terminal and one scan output terminal are arranged at
each of the right- and left-ends. In addition, the
scan output terminal SOL2 and the scan input terminal
25   SIL2 at the left end of the memory macro are connected
by the line 22.

With this configuration, a memory macro scanning

function can be realized by inputting data SI to be
scanned to the scan input terminal SIR1 at the right
end of this memory macro, and outputting scanned data
SO from the scan output terminal SOR1 at the same end.

5   The line 22 cannot be a long line because it
connects the scan output terminal SOL2 and the scan
input terminal SIL2 arranged close to each other at the
left end of the operation control circuit 21.
Therefore, even when the data SI input to the scan

10   input terminal SIR1 is scanned to the scan output
terminal SOR1 to output the data SO, deterioration of
the performance of the scan operation can be
suppressed.

        Next, the arrangement of a memory macro formed by

15   adding an array block 11B to a memory macro having the
array block 11 and the operation control circuit 21
will be explained below. When the operation control
circuit 21 is to be shared by the two array blocks 11
and 11B, these two array blocks 11 and 11B are usually

20   so arranged as to have a mirror inversion relationship
with respect to the operation control circuit 21.

        FIG. 5 is a diagram showing the arrangement of the
memory macro of the second modification of the above
first embodiment.

25   As shown in FIG. 5, this memory macro has the
array block 11, the operation control circuit 21, and
the array block 11B. This array block 11B is the

mirror inversion of the array block 11 with respect to the operation control circuit 21. The configurations of the array block 11 and the operation control circuit 21 are the same as shown in FIG. 4.

5   The configuration of the array block 11B is the mirror inversion of the configuration shown in FIG. 3. FIG. 5 shows only scan input terminals SIR1B and SIL1B and scan output terminals SOL1B and SOR1B in an input/output control circuit. In this input/output

10   control circuit of the array block 11B, 128 IO registers and 128 IO terminals are arranged.

     The scan input terminal SIR1B connected to the scan output terminal SOL2 is placed at the right end of the input/output control circuit of the array block

15   11B. The scan output terminal SOL1B is placed at the left end of this input/output control circuit. 64 series-connected IO registers are arranged between the scan input terminal SIR1B and the scan output terminal SOL1B. These 64 IO registers have latching means

20   capable of scanning, respectively, and thereby form a scan chain. An IO terminal is connected to each of these 64 IO registers.

     The scan input terminal SIL1B is placed at the left end of the array block 11B. The scan output

25   terminal SOR1B connected to the scan input terminal SIL2 is placed at the right end of the array block 11B. 64 series-connected IO registers are arranged between

the scan input terminal SIL1B and the scan output

terminal SOR1B. These 64 IO registers have latching

means capable of scanning, respectively, and thereby

form a scan chain. An IO terminal is connected to each

5   of these 64 IO registers.

Furthermore, a line 24 is connected between the

scan output terminal SOL1B and the scan input terminal

SIL1B.

In the memory macro having this configuration,

10   data SI input to the scan input terminal SIR1 is

scanned in a plurality of series-connected IO registers

in sequence, transferred to the scan output terminal

SOL1, and then to the scan input terminal SIR2. This

data SI transferred to the scan input terminal SIR2 is

15   scanned in a plurality of IO registers, transferred to

the scan output terminal SOL2, and then to the scan

input terminal SIR1B. The data SI is further scanned

in a plurality of series-connected IO registers in

sequence and transferred to the scan output terminal

20   SOL1B.

The data SI transferred to the scan output

terminal SOL1B is input to the scan input terminal

SIL1B through the line 24. This data SI input to the

scan input terminal SIL1B is scanned in a plurality of

25   IO registers in sequence, transferred to the scan

output terminal SOR1B, and then to the scan input

terminal SIL2. The data SI input to the scan input

terminal SIL2 is scanned in a plurality of IO

registers, transferred to the scan output terminal

SOR2, and then to the scan input terminal SIL1. This

data SI is further scanned in a plurality of

5   series-connected IO registers in sequence, transferred

to the scan output terminal SOR1, and output as data

SO.

As described above, one scan input terminal and

one scan output terminal are arranged at the left end

10   of each of the array block 11, the operation control

circuit 21, and the array block 11B. One scan input

terminal and one scan input terminal are also arranged

at the right end of each of the array block 11, the

operation control circuit 21, and the array block 11B.

15   When the array block 11, the operation control circuit

21, and the array block 11B are juxtaposed, the scan

output terminal SOL1 and the scan input terminal SIR2

are connected. In addition, the scan output terminal

SOL2 and the scan input terminal SIR1B are connected,

20   the scan output terminal SOR1B and the scan input

terminal SIL2 are connected, and the scan output

terminal SOR2 and the scan input terminal SIL1 are

connected. Accordingly, even when a memory macro is

constructed by the array block 11, the operation

25   control circuit 21, and the array block 11B, one scan

input terminal and one scan output terminal can be

arranged at each of the right- and left-ends. In

addition, the scan output terminal SOL1B and the scan input terminal SIL1B at the left end of the memory macro are connected by the line 24.

With this configuration, a memory macro scanning function can be realized by inputting data SI to be scanned to the scan input terminal SIR1 at the right end of this memory macro, and outputting scanned data SO from the scan output terminal SOR1 at the same end.

The line 24 cannot be a long line because it connects the scan output terminal SOL1B and the scan input terminal SIL1B arranged close to each other at the left end of the array block 11B. Therefore, even when the data SI input to the scan input terminal SIR1 is scanned to the scan output terminal SOR1 to output the data SO, deterioration of the performance of the scan operation can be suppressed.

A configuration in which two memory macros each having the array block 11 and the operation control circuit 21 shown in FIG. 4 are juxtaposed will be explained below.

FIG. 6 is a diagram showing the arrangement of the memory macros of the third modification of the above first embodiment.

As shown in FIG. 6, a memory macro 31 having the array block 11 and the operation control circuit 21 is juxtaposed with a memory macro 31B as the mirror inversion of this memory macro 31.

The configuration of the memory macro 31 is the same as shown in FIG. 4. FIG. 6 shows only the scan input terminals SIR1 and SIL1 and the scan output terminals SOL1 and SOR1 in the input/output control circuit of the array block 11. FIG. 6 also shows the scan input terminals SIR2 and SIL2 and the scan output terminals SOL2 and SOR2 in the operation control circuit 21.

The configuration of the memory macro 31B is the mirror inversion of the configuration shown in FIG. 4. FIG. 6 shows only the scan input terminals SIR1B and SIL1B and the scan output terminals SOL1B and SOR1B in the input/output control circuit of the array block 11. FIG. 6 also shows scan input terminals SIR2B and SIL2B and scan output terminals SOL2B and SOR2B in the operation control circuit 21.

The scan output terminal SOL2 at the left end of the memory macro 31 is connected to the scan output terminal SIR2B at the right end of the memory macro 31B by a line 32. The scan output terminal SOR2B at the right end of the memory macro 31B is connected to the scan input terminal SIL2 at the left end of the memory macro 31 by a line 33. In addition, the scan output terminal SOL1B and the scan input terminal SIL1B at the left end of the memory macro 31B are connected by a line 34.

The scan input terminal SIR1 at the right end of

the memory macro 31 is an input terminal for input data
SI to be scanned. The scan output terminal SOR1 at the
right end of the memory macro 31 is an output terminal
for scanned output data SO.

5   With this configuration, even when a plurality of
memory macros are juxtaposed, a scan chain can be
readily constructed by connecting adjacent scan output
and input terminals. Since this does not extend the
scan chain, deterioration of the performance of the
10   scan operation can be suppressed.

Also, the lines 32, 33, and 34 for realizing scan
can be formed by an automatic wiring function by
registering, in an automatic wiring tool, the scan
input/output terminals SIR1/SOL2, SOR1/SIL2,
15   SIR2B/SOL1B, and SOR2B/SIL1B arranged at the right- and
left-ends of the memory macros 31 and 31B. This
automatic wiring function can be used even when logic
registers exist in juxtaposed memory macros. This can
increase the degree of freedom of wiring formation.

20   In the first embodiment and its modifications as
described above, it is possible to reduce performance
deterioration of the scan operation caused by the
formation of a long external line, and to eliminate
obstacles to automatization of the scan operation.
25   Second Embodiment

An array block constructing a semiconductor
integrated circuit of the second embodiment of the

present invention will be described below. This second
embodiment differs from the first embodiment in that a
plurality of buffers are arranged between a second scan
input terminal SIL1 and a second scan output terminal

5   SOR1. The rest is the same as the first embodiment.

FIG. 7 is a diagram showing the arrangement of the
array block of the second embodiment.

As shown in FIG. 7, in this array block 41, a
memory cell array 12, a row decoder 13, a column

10   decoder 14, a sense amplifier 15, and an input/output
control circuit 42 are formed.

In the input/output control circuit 42, IO
registers 42A, IO terminals 42B, first and second scan
input terminals SIR1 and SIL1, and first and second

15   scan output terminals SOL1 and SOR1 are arranged.

The first scan input terminal SIR1 is placed at
the right end of the input/output control circuit 42.
The first scan output terminal SOL1 is placed at the
left end of the input/output circuit 42. The

20   series-connected IO registers 42A are arranged between
the first scan input terminal SIR1 and the first scan
output terminal SOL1. These IO registers 42A have
latching means capable of scanning, respectively, and
are connected in series to form a scan chain. The

25   IO terminal 42B is connected to each of these IO
registers 42A.

The second scan input terminal SIL1 is placed at

the left end of the input/output control circuit 42.
The second scan output terminal SOR1 is placed at the
right end of the input/output control circuit 42. A
plurality of series-connected buffers 42C are arranged

5 between the second scan input terminal SIL1 and the
second scan output terminal SOR1. Note that the second
scan input terminal SIL1 is positioned near the first
scan output terminal SOL1, and the second scan output
terminal SOR1 is positioned near the first scan input

10 terminal SIR1.

In addition, a line 43 is connected between the
first scan output terminal SOL1 and the second scan
input terminal SIL1.

In the array block 41 having this configuration,

15 input data to the scan input terminal SIR1 is scanned
in the series-connected IO registers 42A in sequence,
and transferred to the scan output terminal SOL1. The
data transferred to the scan output terminal SOL1 is
input to the scan input terminal SIL1 through the line

20 43. This data input to the scan input terminal SIL1 is
further transferred to the scan output terminal SOR1
through the series-connected buffers 42C.

As described above, the scan input terminal SIR1
is placed at the right end of the array block 41, and

25 the scan output terminal SOL1 as an output of this scan
input terminal SIR1 is placed at the left end of the
array block 41. Also, the scan input terminal SIL1 is

placed at the left end of the array block 41, and the scan output terminal SOR1 as an output of this scan input terminal SIL1 is placed at the right end of the array block 41. The scan output terminal SOL1 and the

5   scan input terminal SIL1 arranged at the left end of the array block 41 are connected by the line 43. Accordingly, a scan chain can be formed between the scan input terminal SIR1 and the scan output terminal SOR1, so data input to the scan input terminal SIR1 can

10   be scanned to the scan output terminal SOR1.

The line 43 cannot be a long line because it connects the scan output terminal SOL1 and the scan input terminal SIL1 arranged close to each other. Therefore, even when data input to the scan input

15   terminal SIR1 is scanned to the scan output terminal SOR1, deterioration of the performance of the scan operation can be suppressed.

In the second embodiment as described above, it is possible to reduce performance deterioration of the

20   scan operation caused by the formation of a long external line, and to eliminate obstacles to automatization of the scan operation.

Third Embodiment

An array block constructing a semiconductor

25   integrated circuit of the third embodiment of the present invention will be described below. This third embodiment differs from the first embodiment in that a

scan input terminal and scan output terminal are formed
near one end of the array block, and IO registers are
connected by a line without forming any scan input and
output terminals at the other end. The rest is the

5   same as the first embodiment.

FIG. 8 is a diagram showing the arrangement of the
array block of the third embodiment.

As shown in FIG. 8, in this array block 51, a
memory cell array 12, a row decoder 13, a column

10   decoder 14, a sense amplifier 15, and an input/output
control circuit 52 are formed.

In the input/output control circuit 52, IO
registers 52A, IO terminals 52B, IO terminals 52C, a
scan input terminal SIL1, and a scan output terminal

15   SOL1 are arranged.

At the left end of the input/output control
circuit 52, the scan input terminal SIL1 and the scan
output terminal SOL1 are arranged. One end of the
series-connected IO registers 52A is connected to the

20   scan input terminal SIL1. These IO registers 52A are
arranged from the left end to the right end of the
input/output control circuit 52.

Also, the IO registers 52B are connected in series
and arranged from the right end to the left end of the

25   input/output control circuit 52. The other end of the
IO registers 52A is connected to one end of the IO
registers 52B. The other end of the IO registers 52B

is connected to the scan output terminal SOL1.

These IO registers 52A and 52B have latching means capable of scanning, respectively, and thereby form a scan chain. The IO terminal 52C is connected to each of these IO registers 52A and 52B. Note that the scan input terminal SIL1 is placed near the scan output terminal SOL1.

In the array block 51 having this configuration, input data to the scan input terminal SIL1 is scanned in the series-connected IO registers 52A and 52B in sequence, and transferred to the scan output terminal SOL1.

As described above, the scan input terminal SIL1 is placed at the left end of the array block 51, and the scan output terminal SOL1 as an output of this scan input terminal SIL1 is also placed at the left end of the array block 51. Between the scan input terminal SIL1 and the scan output terminal SOL1, the IO registers 52A and 52B are connected in series. Accordingly, a scan chain can be formed between the scan input terminal SIL1 and the scan output terminal SOL1, so data input to the scan input terminal SIL1 can be scanned to the scan output terminal SOL1.

As described above, on scan input terminal and one scan output terminal are formed near one end of an array block. Therefore, even when memory macros having various configurations are formed, it is possible to

suppress performance deterioration of the scan
operation caused by the formation of a long external
line. In addition, since no lines need be formed
outside the memory macro, obstacles to automatization
5   of the scan operation can be eliminated.

The arrangement of a memory macro in which an
operation control circuit is formed in the array block
51 will be described below.

FIG. 9 is a diagram showing the arrangement of a
10   memory macro of the first modification of the third
embodiment described above.

As shown in FIG. 9, this memory macro has the
array block 51 shown in FIG. 8 and an operation control
circuit 61. The internal configuration of the array
15   block 51 is the same as shown in FIG. 8. FIG. 9 shows
only the scan input terminal SIL1 and the scan output
terminal SOL1 in the input/output control circuit 52.
In this input/output control circuit of the array block
51, 128 IO registers and 128 IO terminals are arranged.

20   That is, the scan input terminal SIL1 and the scan
output terminal SOL1 are arranged at the left end of
the input/output control circuit of the array block 51.
The 128 IO registers connected in series as shown in
FIG. 8 are arranged between the scan input terminal
25   SIL1 and the scan output terminal SOL1. These 128 IO
registers have latching means capable of scanning,
respectively, and thereby form a scan chain. An IO

terminal is connected to each of these 128 IO registers.

A scan input terminal SID2 is placed at the lower end of the operation control circuit 61. At the right end of this operation control circuit 61, a scan output terminal SOR2 connected to the scan input terminal SID2 and to the scan input terminal SIL1 is placed.

A scan input terminal SIR2 connected to the scan output terminal SOL1 is placed at the right end of the operation control circuit 61. A scan output terminal SOL2 is placed at the left end of the operation control circuit 61. A plurality of IO registers are connected between the scan input terminal SIR2 and the scan output terminal SOL2. These IO registers have latching means capable of scanning, respectively, and thereby form a scan chain. An IO terminal (not shown) is connected to each of these IO registers. This IO terminal inputs and outputs a control signal CNT.

A scan input terminal SIL2 is placed at the left end of the operation control circuit 61. A scan output terminal SOD2 connected to the scan output terminal SIL2 is placed at the lower end of the operation control circuit 61. This scan output terminal SOD2 is positioned near the scan input terminal SID2.

The scan input terminal SID2 at the lower end is for extracting the scan output terminal SOR2 at the right end to the lower end, so the scan input terminal

SID2 and the scan output terminal SOR2 are merely
connected by a line. Likewise, the scan output
terminal SOD2 at the lower end is for extracting the
scan input terminal SIL2 at the left end to the lower
5   end, so the scan output terminal SOD2 and the scan
input terminal SIL2 are merely connected by a line.
Hence, all IO registers in the operation control .
circuit 61 are arranged between the scan input terminal
SIR2 and the scan output terminal SOL2.

10   In the memory macro having this configuration,
data SI input to the scan input terminal SID2 is
transferred to the scan output terminal SOR2 and then
to the scan input terminal SIL1. This data SI
transferred to the scan input terminal SIL1 is scanned
15   in a plurality of series-connected IO registers in
sequence, transferred to the scan output terminal SOL1,
and then to the scan input terminal SIR2. The data SI
is further scanned in a plurality of IO registers and
transferred to the scan output terminal SOL2.

20   In the above memory macro, when the array block 51
and the operation control circuit 61 are juxtaposed,
the scan output terminal SOR2 and the scan input
terminal SIL1 are connected, and the scan output
terminal SOL1 and the scan input terminal SIR2 are
25   connected.

With this configuration, a memory macro scanning
function can be realized by inputting data SI to be

scanned to the scan input terminal SID2 at the lower end of this memory macro, and outputting scanned data SO from the scan output terminal SOL2 at the left end of the memory cell. Since this memory macro functions

5   as one scan chain, no external line need be connected. This reduces limitations on design, facilitates handling of this memory macro, and can also suppress performance deterioration of the scan operation. In addition, since no lines need be formed outside the

10   memory macro, obstacles to automatization of the scan operation can be eliminated.

The arrangement of a memory macro formed by adding an array block 51B to a memory macro having the array block 51 and the operation control circuit 61 will be

15   explained below. When the operation control circuit 61 is to be shared by the two array blocks 51 and 51B, these two array blocks 51 and 51B are usually so arranged as to have a mirror inversion relationship with respect to the operation control circuit 61.

20   FIG. 10 is a diagram showing the arrangement of the memory macro of the second modification of the above third embodiment.

As shown in FIG. 10, this memory macro has the array block 51, the operation control circuit 61, and

25   the array block 51B. This array block 51B is the mirror inversion of the array block 51 with respect to the operation control circuit 61. The configurations

of the array block 51 and the operation control circuit
61 are the same as shown in FIG. 9.

The configuration of the array block 51B is the
mirror inversion of the configuration shown in FIG. 8.
FIG. 10 shows only a scan input terminal SIR1B and a
scan output terminal SOR1B in an input/output control
circuit. In this input/output control circuit of the
array block 51B, 128 IO registers and 128 IO terminals
are arranged.

The scan input terminal SIR1B connected to the
scan output terminal SOL2 is placed at the right end of
the input/output control circuit of the array block
51B. Similarly, the scan output terminal SOR1B
connected to the scan input terminal SIL2 is placed at
the right end of this input/output control circuit.
Between the scan input terminal SIR1B and the scan
output terminal SOR1B, the 128 IO registers connected
in series as shown in FIG 8 are arranged. These 128 IO
registers have latching means capable of scanning,
respectively, and thereby form a scan chain. An IO
terminal is connected to each of these 128 IO
registers.

In the memory macro having this configuration,
data SI input to the scan input terminal SID2 is
transferred to the scan output terminal SOR2 and then
to the scan input terminal SIL1. This data SI
transferred to the scan input terminal SIL1 is scanned

in a plurality of series-connected IO registers in
sequence, transferred to the scan output terminal SOL1,
and then to the scan input terminal SIR2. The data SI
is further scanned in a plurality of series-connected

5   IO registers, transferred to the scan output terminal
SOL2, and then to the scan input terminal SIR1B.

The data SI transferred to the scan output
terminal SIR1B is scanned in a plurality of
series-connected IO registers in sequence, transferred

10   to the scan output terminal SOR1B, and then to the scan
input terminal SIL2. Furthermore, the data SI input to
the scan input terminal SIL2 is transferred to the scan
output terminal SOD2.

In the above memory macro, when the array block

15   51, the operation control circuit 61, and the array
block 51B are juxtaposed, the scan output terminal SOR2
and the scan input terminal SIL1 are connected. In
addition, the scan output terminal SOL1 and the scan
input terminal SIR2 are connected, the scan output

20   terminal SOL2 and the scan input terminal SIR1B are
connected, and the scan output terminal SOR1B and the
scan input terminal SIL2 are connected.

With this configuration, a memory macro scanning
function can be realized by inputting data SI to be

25   scanned to the scan input terminal SID2 at the lower
end of this memory macro, and outputting scanned data
SO from the scan output terminal SOD2 at the same end.

Since this memory macro functions as one scan chain, no external line need be connected. This reduces limitations on design, facilitates handling of this memory macro, and can also suppress performance

5 deterioration of the scan operation. In addition, since no lines need be formed outside the memory macro, obstacles to automatization of the scan operation can be eliminated.

In the third embodiment and its modifications as
10 described above, it is possible to reduce performance deterioration of the scan operation caused by the formation of a long external line, and to eliminate obstacles to automatization of the scan operation.
Fourth Embodiment

15 An array block constructing a semiconductor integrated circuit of the fourth embodiment of the present invention will be described below. In this fourth embodiment, to eliminate data through by hold violation between IO registers in an array block, a
20 buffer for delaying a clock signal supplied to a preceding IO register is formed. The rest is the same as the array block configuration of the second embodiment. In addition, in this fourth embodiment, the array blocks described above are arranged to have a
25 mirror inversion relationship with respect to an operation control circuit.

FIG. 11 is a diagram showing the arrangement of

the memory macro of the fourth embodiment.

As shown in FIG. 11, this memory macro 71 has an array block 72, an operation control circuit 21, and an array block 72B. This array block 72B is the mirror inversion of the array block 72 with respect to the operation control circuit 21.

The internal configuration of the array block 72 is the same as the array block 11 shown in FIG. 3 except for an input/output control circuit 16. That is, the array block 72 has a memory cell array 12, a row decoder 13, a column decoder 14, and a sense amplifier 15. Therefore, only the internal arrangement of the input/output control circuit will be described below.

This input/output control circuit of the array block 72 has a plurality of IO registers 73 to each of which an IO terminal is connected, a plurality of buffers 75 and 76, a first scan input terminal SIR3, a first scan output terminal SOL3, a second scan input terminal SIL3, and a second scan output terminal SOR3.

The first scan input terminal SIR3 is placed at the right end of the array block 72. The first scan output terminal SOL3 is placed at the left end of the array block 72. A plurality of (e.g., 128) series-connected IO registers 73 are arranged between the first scan input terminal SIR3 and the first scan output terminal SOL3. These IO registers 73 have

latching means capable of scanning, respectively, and are connected in series to form a scan chain.

A clock signal SSCLK is input to the IO register 73 in the output stage. A clock signal SSCLK passing through the buffer 75 is input to the IO register 73 in the input stage. This clock signal SSCLK is supplied from the operation control circuit 21. A plurality of (e.g., 128) IO terminals are connected to these IO registers 73.

The second scan input terminal SIL3 is placed at the left end of the array block 72. The second scan output terminal SOR3 is placed at the right end of the array block 72. A plurality of series-connected buffers 76 are arranged between the second scan input terminal SIL3 and the second scan output terminal SOR3. Note that the second scan input terminal SIL3 is positioned near the first scan output terminal SOL3, and the second scan output terminal SOR3 is positioned near the first scan input terminal SIR3.

The configuration of the array block 72B is the mirror inversion of the array block 72. That is, a plurality of (e.g., 128) series-connected IO registers 73B are arranged between a scan input terminal SIL3B and a scan output terminal SOR3B. These IO registers 73B have latching means capable of scanning, respectively, and are connected in series to form a scan chain.

A clock signal SSCLK is input to the IO register
73B in the output stage. A clock signal SSCLK passing
through a buffer 75B is input to the IO register 73B in
the input stage. This clock signal SSCLK is supplied
5   from the operation control circuit 21. A plurality of
(e.g., 128) IO terminals are connected to these IO
registers 73B.

Also, a plurality of series-connected buffers 76B
are arranged between the scan input terminal SIL3B and
10   the scan output terminal SOL3B. Note that the scan
input terminal SIR3B is positioned near the scan output
terminal SOR3B, and the scan output terminal SOL3B is
positioned near the scan input terminal SIL3B. In
addition, a line 77 is connected between the scan
15   output terminal SOL3B and the scan input terminal
SIL3B.

The arrangement of the operation control circuit
21 is the same as shown in FIG. 4.

In the memory macro 71, no IO registers but only
20   the buffers 76 and 76B are present in the path from the
scan input terminal SIL3 to the scan output terminal
SOR3 and in the path from the scan input terminal SIR3B
to the scan output terminal SOL3B, respectively. Also,
the IO registers 73 and 73B are present in the path
25   from the scan input terminal SIR3 to the scan output
terminal SOL3 and in the path from the scan input
terminal SIL3B to the scan output terminal SOR3B,

respectively.

The clock signal SSCLK described above is a clock signal for scan shift. In response to this clock signal, the IO registers 73 and 73B output stored data to subsequent IO registers.

In the memory macro 71 having this configuration, data SI input to the scan input terminal SIR3 is scanned in the series-connected IO registers 73 in sequence, transferred to the scan output terminal SOL3, and then to the scan input terminal SIR2. During the scan, an undelayed clock signal SSCLK is supplied to the IO register 73 in the subsequent stage (data receiving side), and a clock signal SSCLK delayed by the buffer 75 is supplied to the IO register 73 in the preceding stage (data transferring side). Consequently, data stored in the subsequent IO register 73 is transferred before data stored in the preceding IO register 73 is transferred. In this manner, "data through" by hold violation is prevented.

The data SI transferred to the scan input terminal SIR2 is scanned in a plurality of IO registers, transferred to the scan output terminal SOL2, and then to the scan input terminal SIR3B. This data SI transferred to the scan input terminal SIR3B is transferred to the scan output terminal SOL3B through the series-connected buffers 76B.

The data SI transferred to the scan output

terminal SOL3B is input to the scan input terminal
SIL3B through the line 77. This data SI input to
the scan input terminal SIL3B is scanned in the
series-connected IO registers 73B in sequence,

5 transferred to the scan output terminal SOR3B, and then
to the scan input terminal SIL2. During the scan, in
the same manner as described above, an undelayed clock
signal SSCLK is supplied to the IO register 73B in the
subsequent stage, and a clock signal SSCLK delayed by

10 the buffer 75B is supplied to the IO register 73B in
the preceding stage. Consequently, data stored in the
subsequent IO register 73B is transferred before data
stored in the preceding IO register 73B is transferred.
In this way, "data through" by hold violation is

15 prevented.

The data SI input to the scan input terminal SIL2
is scanned in a plurality of IO registers, transferred
to the scan output terminal SOR2, and then to the scan
input terminal SIL3. This data SI is further

20 transferred to the scan output terminal SOR3 through
the series-connected buffers 76. As a consequence,
data SO scanned in the memory macro 71 is output from
the scan output terminal SOR3.

In this fourth embodiment as described above, an

25 IO register in the succeeding stage in the data shift
direction receives a clock signal before an IO register
in the preceding stage. Therefore, this succeeding IO

register can receive data transferred from the preceding IO register. This can eliminate "data through" by hold violation. This embodiment is an example which facilitates shift clock design for IO

5 registers.

In each of the above embodiments, a scan input terminal and a scan output terminal are formed at the left- and right ends. However, as shown in FIG. 12, it is also possible to form a scan input terminal SIL and

10 a scan output terminal SOL at the left end, a scan input terminal SIR and a scan output terminal SOR at the right end, a scan input terminal SIU and a scan output terminal SOU at the upper end, and a scan input terminal SID and a scan output terminal SOD at the

15 lower end.

In the embodiments of the present invention as have been described above, it is possible to provide a semiconductor integrated circuit which, when a scan function is set for memory macros having various

20 configurations, can reduce performance deterioration of the scan operation caused by the formation of a long external line, and can eliminate obstacles to automatization of the scan operation by eliminating lines formed outside a memory macro.

25 Also, the individual embodiments described above can be practiced not only singly but also in combination.

Furthermore, the above-mentioned embodiments include inventions in various stages. So, inventions in various stages can be extracted by appropriately combining a plurality of constituent elements disclosed in the embodiments.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit and scope of the general inventive concept as defined by the appended claims and their equivalents.